

What Is Claimed Is:

1 1. A method for enhancing effective timing margins and reliability of
2 a digital system bus, comprising:
3 monitoring the digital system bus to determine a data flow between
4 devices on the digital system bus; and
5 if an absence of data flow between devices on the digital system bus is
6 detected;
7 generating a pseudo-data signal, and
8 transmission the pseudo-data signal on the digital system
9 bus, in order to keep the digital system bus active so that
10 subsequent transmissions do not suffer from effects caused by an
11 inactive digital system bus.

1 2. The method of claim 1, further comprising terminating the pseudo-
2 data signal abruptly when the digital system bus is needed to transmit real data.

1 3. The method of claim 1, wherein the pseudo-data signal is a pre-
2 determined pattern sequence.

1 4. The method of claim 1, wherein the pseudo-data signal is a
2 continually changing pattern sequence generated by a pseudo-random generator.

1 5. The method of claim 1, wherein the pseudo-data signal is a
2 continually changing pattern sequence generated based on previous transitions on
3 the digital system bus to maintain a substantially equal number of high and low
4 transitions on the digital system bus.

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1 6. The method of claim 1, further comprising directing the pseudo-
2 data signal to a trash bin address, wherein the trash bin address is not used by
3 devices on the digital system bus.

1 7. The method of claim 1, further comprising generating an idle
2 command in conjunction with the pseudo-data signal, wherein the idle command
3 informs devices on the digital system bus not to use the pseudo-data signal.

1 8. An apparatus that facilitates enhancing effective timing margins
2 and reliability of a digital system bus, comprising:
3 a monitoring mechanism that is configured to monitor the digital system
4 bus to determine a data flow between devices on the digital system bus;
5 a generating mechanism that is configured to generate a pseudo-data signal
6 if an absence of data flow between devices on the digital system bus is detected;
7 and
8 a transmission mechanism that is configured to broadcast the pseudo-data
9 signal on the digital system bus, in order to keep the digital system bus active so
10 that subsequent transmissions do not suffer from effects caused by an inactive
11 digital system bus.

1 9. The apparatus of claim 8, further comprising a terminating
2 mechanism that is configured to terminate the pseudo-data signal abruptly when
3 the digital system bus is needed to transmit real data.

1 10. The apparatus of claim 8, wherein the pseudo-data signal is a pre-
2 determined pattern sequence.

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3 voltage changes associated with a first pulse after an idle period on the digital
4 system bus.

1 17. The apparatus of claim 8, wherein effects caused by the inactive
2 digital system bus include a power supply effect associated with the digital system
3 bus returning to a constant load level after an idle period on the digital system bus.

1 18. The apparatus of claim 8, wherein effects caused by the inactive
2 digital system bus include a transmission line mis-matching effect associated with
3 signal reflections on the digital system bus caused by mis-matched impedance on
4 the digital system bus.

1 19. The apparatus of claim 8, wherein effects caused by the inactive
2 digital system bus include temperature effects associated with signal driver
3 transistors being held in a constant state of conduction during an idle period on the
4 digital system bus.

1 20. The apparatus of claim 8, wherein the generating mechanism is
2 further configured to generate the pseudo-data signal in a manner such that
3 crosstalk is minimized across the digital system bus.

1 ~~21.~~ A computer system that facilitates enhancing effective timing
2 margins and reliability of a digital system bus, comprising:
3 a central processor unit coupled to the digital system bus;
4 a memory subsystem coupled to the digital system bus;

1 a monitoring mechanism that is configured to monitor the digital system
2 bus to determine a data flow between the central processor unit and the memory
3 subsystem on the digital system bus;
4 a generating mechanism that is configured to generate a pseudo-data signal
5 if an absence of data flow between the central processor unit and the memory
6 subsystem is detected; and
7 a transmission mechanism that is configured to broadcast the pseudo-data
8 signal on the digital system bus, in order to keep the digital system bus active so
9 that subsequent transmissions between the central processor unit and the memory
10 subsystem do not suffer from effects caused by an inactive digital system bus.

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FOOTNOTES